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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/595,461	SMEDLEY ET AL.	
	Examiner	Art Unit	
	EMILY PHAM	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01/12/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-23* is/are allowed.

6)☒ Claim(s) *1-14,24-39,40-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/26/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/26/2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. Figures 1A - 4B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 4 is objected to because of the following informalities: "… further comprising connecting first second and third voltage signals such that …", proper punctuation is required.

4. Claim 39 is objected to because claim 39 recites the limitation "the third voltage source" in line 16. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Jacobs et al. (USP 6,046,915).

Regarding independent claim 1: Jacobs et al. **(FIG 13 – FIG 17)** disclose a method of modulating a three-phase three-level power converter **(1300, 1400, 1500, 1600, 1700)** comprising a first **(Va)**, a second **(Vb)** and a third voltage **(Vc)** source, each voltage source being configured to output a time-varying signal and being inductively coupled to a separate input node **(inherently)**, each input node being connectable to a first output node, a second output node and a third output node, the converter further comprising a first capacitive element **(1314, 1414, 1514, 1614, 1714)** coupled between the first and the second output nodes and a second capacitive element **(1315, 1415, 1515, 1615, 1715)** coupled between the second output node and the third output node, wherein each time-varying voltage signal **(VAC with phase A, B, and C)** has substantially the same period and a different phase, the method comprising: determining which voltage signal has the highest voltage, the lowest voltage and the intermediate voltage higher than one of the voltage signals and lower than the other voltage signal for each of a plurality of sub-periods **(col. 3, lines 1-8)**; connecting the voltage signal having the intermediate voltage to only the first output node during each

sub-period **(FIG 4; col. 6, line 56 – col. 7, line 34)**; connecting the voltage signal having the highest voltage to one of the second or third output nodes during each sub-period; and connecting the voltage signal having the lowest voltage to one of the second or third output nodes during each sub-period **(FIG 4; col. 6, line 56 – col. 7, line 34)**.

Regarding independent claim 9: Jacobs et al. disclose **(FIG 13 – FIG 17)** a method of modulating a three-phase three-level power converter **(1300, 1400, 1500, 1600, 1700)**, comprising: providing a power converter comprising a first **(Va)**, a second **(Vb)** and a third voltage **(Vc)** source each configured to output a time-varying signal **(VAC with phase A, B, and C)**, the first **(Va)** and second **(Vb)** voltage sources each being inductively coupled to a separate input node **(inherently)**, the output nodes being connectable to a first and second output node, and the third voltage source being inductively coupled to a third output node, the power converter further comprising a first capacitive element **(1314, 1414, 1514, 1614, 1714)** coupled between the first and the second output node, and a second capacitive element **(1315, 1415, 1515, 1615, 1715)** coupled between the second output node and the third output node, wherein each time-varying voltage signal has substantially the same period and a different phase **(FIG 4, phase A, B, and C)**; and providing a controller **(switches)** configured to control the connection of the second and third voltage sources to the second and third output nodes.

Regarding dependent claim 10: Jacobs et al. **(FIG 16)** disclose the method wherein the input nodes are connectable to the first and second output nodes with a plurality of switching elements **(1625, 1626, 1628)**.

7. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Weng et al. (USP 6,239,995).

Weng et al. disclose **(FIG 2)** a method of modulating a three-phase three-level power converter, comprising: providing a power converter comprising a first **(VA)**, a second **(VB)** and a third voltage **(VC)** source each configured to output a time-varying signal **(VAC with phase A, B, and C)**, the first **(VA)** and second **(VB)** voltage sources each being inductively coupled to a separate input node **(coupled via La and Lb)**, the output nodes being connectable to a first and second output node, and the third voltage source **(VC)** being inductively coupled to a third output node **(Lc)**, the power converter further comprising a first capacitive element **(Cdc1)** coupled between the first and the second output node, and a second capacitive element **(Cdc2)** coupled between the second output node and the third output node, wherein each time-varying voltage signal has substantially the same period and a different phase **(FIG 4, phase A, B, and C)**; and providing a controller **(110)** configured to control the connection of the second and third voltage sources to the second and third output nodes.

8. Claims 27-32, 36-38, 43-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Smedley et al. (USP 6,297,980 - cited in IDS).

Regarding independent claim 27: Smedley et al. **(FIG 7, FIG 8)** disclose a three phase three level universal controller, comprising: a one cycle control (OCC) core **(Low**

Pass Filters, multiplexers, comparators, flip-flops) configured to generate a plurality of drive signals **(plurality signals from LOGIC)**; a region selection unit **(Region Selection Circuit)** configured to monitor a first **(Va)**, second **(Vb)** and third **(Vc)** main time-varying voltage signal, each voltage signal having a different phase **(A, B, C)**, and configured to determine a region of operation based on each of the main signals **(Va, Vb, Vc)**; an signal selection unit **(the component with ILp and ILn as outputs)** coupled with the region selection unit **(Region Selection Circuit)** and the OCC core and configured to select one or more input signals based on the region of operation and provide the selected signals to the core; and a drive signal distribution unit coupled to the OCC core and the region selection unit, the drive signal distribution unit configured to distribute the drive signals to an active power filter (APF), wherein the drive signals are configured to control a plurality of switching elements in the APF **(col. 6, line 35 – col. 8, line 9)**.

Regarding dependent claim 28: Smedley et al. **(FIG 7, FIG 8)** disclose the universal controller, further comprising a reference signal source unit configured to provide a reference signal to the control core **(col. 2, lines 22-30)**.

Regarding dependent claim 29: Smedley et al. **(FIG 7, FIG 8)** disclose the universal controller, wherein the signal selection unit **(the component with ILp and ILn as outputs)** is configured to combine the reference signal with each of the time varying voltage signals and select one or more input signals from the combined signals.

Regarding independent claim 30: Smedley et al. **(FIG 9, FIG 10)** disclose a three phase three level universal controller, comprising: a one cycle control (OCC) core **(Low**

Pass Filters, multiplexers, comparators, flip-flops) configured to generate a plurality of drive signals **(plurality signals from LOGIC)**; a region selection unit **(Region Selection Circuit)** configured to monitor a first **(Va)**, second **(Vb)** and third **(Vc)** main time-varying voltage signal, each voltage signal having a different phase **(A, B, C)**, and configured to determine a region of operation based on each of the main signals **(Va, Vb, Vc)**; an signal selection unit **(the component with ILp and ILn as outputs)** coupled with the region selection unit **(Region Selection Circuit)** and the OCC core and configured to select one or more input signals based on the region of operation and provide the selected signals to the core; and a drive signal distribution unit coupled to the OCC core and the region selection unit, the drive signal distribution unit configured to distribute the drive signals to an grid connected inverter (GCI), wherein the drive signals are configured to control a plurality of switching elements in the GCI **(col. 8, lines 15 - col. 9, line 34)**.

Regarding dependent claim 31: Smedley et al. **(FIG 9, FIG 10)** disclose the universal controller, further comprising a reference signal source unit configured to provide a reference signal to the control core **(col. 2, lines 22-30)**.

Regarding dependent claim 32: Smedley et al. **(FIG 9, FIG 10)** disclose the universal controller, wherein the signal selection unit **(the component with ILp and ILn as outputs)** is configured to combine the reference signal with each of the time varying voltage signals and select one or more input signals from the combined signals.

Regarding independent claim 36: Smedley et al. disclose a method of modeling a power converter system, comprising: determining a phase offset value and a gain value

for a reference signal, wherein the reference signal is input to a controller model configured to control a power converter; modeling the reference signal by applying the determined phase and gain values into the formula [i aref i bref i cref] = G e e j .theta. .function. [v a v b v c] **(col. 5, line 4)** where: G.sub.e is the gain value **(1/Re)**, .theta. is the phase offset value **(value of 1)**, V.sub.a, V.sub.b and V.sub.c are input signals to the power converter and i.sub.aref **(ia)**, i.sub.bref **(ib)** and i.sub.cref **(ic)** are the reference signals corresponding to V.sub.a **(va)**, V.sub.b **(vb)** and V.sub.c **(vc)**; and modeling the controller with the reference signal generated by the formula.

Regarding independent claim 37: Smedley et al. **(FIG 7)** disclose a three phase three level universal controller, comprising: a one cycle control (OCC) core **(Low Pass Filters, multiplexers, comparators, flip-flops)** configured to generate a plurality of drive signals **(plurality signals from LOGIC)**, the OCC core comprising: a signal adjustment unit **(the component with ILp and ILn as outputs)** configured to condition a plurality of input signals and output a first and a second conditioned signals; an integrator **(AV(S))** configured to integrate an output voltage signal from a power converter and output an integrated signal; a first **(38)** and a second **(41)** comparator each communicatively coupled with the integrator **(AV(S))** and the signal adjustment unit **the component with ILp and ILn as outputs)**, the first comparator **(38)** configured to compare the first conditioned signal with the integrated signal and output a first compared signal and the second comparator **(41)** configured to compare the second conditioned signal with the integrated signal and output a second compared signal; a first flip-flop **(first flip-flop)** communicatively coupled with the first comparator **(38)** and

a clock signal generator **(CLK)** and configured to output a first drive signal; and a second flip-flop **(second flip-flop)** communicatively coupled with the first comparator **(38)** and a clock signal generator **(CLK)** and configured to output a second drive signal, wherein the first and second drive signals are configured to directly control the power converter independent of an operating region of the power converter.

Regarding dependent claim 38: Smedley et al. disclose the first flip-flop and second flip-flops are S/R flip-flops **(flip-flops)**.

Regarding independent claim 43: Smedley et al. disclose **(FIG 5 – FIG 10)** a method of generating a reference signal for a power converter to stabilize performance over a range of load conditions, comprising: scaling down a first, second and third main line voltage signal, wherein each voltage signal has a different phase; inputting these scaled down signals as reference signals to a power converter; and operating the power converter **(col. 1, line 20 – col. 4, line 12)**.

Regarding dependent claim 44: Smedley et al. **(FIG 5 – FIG 10)** disclose the method, wherein the first, second and third main line voltage signals are scaled down from the voltage signal levels present under a substantial load.

Regarding dependent claim 45: Smedley et al. disclose the method, wherein the power converter is a power factor corrected (PFC) rectifier **(col. 5, line 1 – col. 6, line 20)**.

Regarding dependent claim 46: Smedley et al. disclose the method, wherein the power converter is an active power filter (APF) **(col. 6, line 35 – col. 7, line 54)**.

9. Claim 48 is rejected under 35 U.S.C. 102(b) as being anticipated by Jansen (USP 6,160,725). Jansen discloses a method of modulating a switching frequency in a power converter **(Abstract)**, comprising: providing a controller configured to control a power converter having a nonlinear load **(col. 5, lines 11-24)** having a load level, wherein the controller has an input voltage switching frequency; changing the switching frequency in response to a change in the load level of the power converter, wherein the switching frequency is increased when the load level decreases and the switching frequency is decreased when the load level is increased **(col. 7, lines 47-61)**.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. (USP 6,046,915), as applied to claim 1 above, in view of Schierling et al. (USP 6,760,239).

Regarding dependent claim 2: Jacobs et al. disclose the claimed invention except that the input node of the first voltage source is connectable to the first output node with a first switching element, to the second output node with a second switching element and to the third output node with a third switching element, the input node of the second voltage source is connectable to the first output node with a fourth switching

element, to the second output node with a fifth switching element and to the third output node with a sixth switching element, and the input node of the third voltage source is connectable to the first output node with a seventh switching element, to the second output node with an eighth switching element and to the third output node with a ninth switching element. Schierling et al. **(FIG 1)** teach the input node **(1)** of the first voltage source is connectable to the first output node **(1)** with a first switching element **(S11)**, to the second output node **(2)** with a second switching element **(S12)** and to the third output node **(3)** with a third switching element **(S13)**, the input node **(2)** of the second voltage source is connectable to the first output node **(1)** with a fourth switching element **(S21)**, to the second output node **(2)** with a fifth switching element **(S22)** and to the third output node **(3)** with a sixth switching element **(S23)**, and the input node **(3)** of the third voltage source is connectable to the first output node **(1)** with a seventh switching element **(S31)**, to the second output node **(2)** with an eighth switching element **(S32)** and to the third output node **(3)** with a ninth switching element **(S33)**.

Jacobs et al. and Schierling et al. disclose power converter. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the phase selection circuit disclosed by Jacobs et al. with the matrix control circuit taught by Schierling et al. to significantly reduce the switching losses of a matrix converter by dividing switching states into regulated time intervals, placing them into one to one correspondence with the output phase related states, and combining the output phase related states with associated time intervals into a pulse train of

modulation period, so that the sequential commutation always occurs to a nearest input voltage.

Regarding dependent claim 3: Schierling et al. **(FIG 2)** teach the period of the time-varying voltage signals is dividable into six substantially equal sub-periods.

Regarding dependent claim 4: Jacobs et al. disclose the method comprising connecting the first second and third voltage signals such that the voltage at the second output node is the voltage of the signal having the highest voltage and the voltage at the third output node is the voltage of the signal having the lowest voltage **(col. 3, lines 1-8)**.

Regarding dependent claim 5: Jacobs et al. **(FIG 16)** disclose the method comprising providing a universal controller configured to generate a plurality of drive signals, each drive signal configured to control a switching element.

12. Claims 6, 7, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. (USP 6,046,915) as applied to claims 1 and 9 above, in view of Chapuis (USP 6,933,709).

Regarding dependent claims 6 and 12: Jacobs et al. disclose claimed invention except that the universal controller comprises an average current mode control core. Chapuis teaches the universal controller comprises an average current mode control core **(col. 4, lines 44-45)**.

Regarding dependent claims 7 and 13: Jacobs et al. disclose claimed invention except that the universal controller comprises a current mode control core. Chapuis

teaches the universal controller comprises a current mode control core **(col. 4, lines 44-45)**.

Jacobs et al. and Chapuis disclose switching power supply circuit. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the phase selection circuit disclosed by Jacobs et al. with average current mode controller taught by Chapuis to regulate the output current at a desired level.

13. Claims 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. (USP 6,046,915) as applied to claims 1 and 9 above, in view of Marwali (USP 6,466,465).

Regarding dependent claim 8: Jacobs et al. disclose claimed invention except that the universal controller comprises a sliding mode control core. Marwali teaches universal controller comprises a sliding mode control core **(col. 3, lines 25-27)**.

Jacobs et al. and Marwali disclose power supply circuit. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the phase selection circuit disclosed by Jacobs et al. with the inverter taught by Marwali to map the magnitudes of each of three phases into single rotating vectors in two-dimensional space for a fast and no-overshoot response.

14. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobs et al. (USP 6,046,915), as applied to claim 9 above, in view of Athari (USP 7,068,016).

Jacobs et al. disclose the claimed invention except that the universal controller comprises a one-cycle control core. Athari **(FIG 2)** teaches a one-cycle control core **(20)**.

Jacobs et al. and Athari disclose power supply converter. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the phase selection circuit disclosed by Jacobs et al. with one-cycle control PFC converter taught by Athari for th purpose of increasing the effectiveness and reducing the complexity of the controller because OCC technique does not require line voltage sensing and does not need a complicated multiplier circuit.

15. Claims 24-26, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley et al. (USP 6,297,980 - cited in IDS) in view of Bergmann (USP 5,672,957).

Regarding independent claims 24 and 33: Smedley et al. **(FIG 7)** disclose a three phase two/three level universal controller, comprising: a one cycle control (OCC) core **(Low Pass Filters, multiplexers, comparators, flip-flops)** configured to generate a plurality of drive signals **(plurality signals from LOGIC)**; a region selection unit **(Region Selection Circuit)** configured to monitor a first **(Va)**, second **(Vb)** and third **(Vc)** time-varying voltage signal, each voltage signal having a different phase **(A, B, C)**, and configured to determine a region of operation based on each of the time-varying signals **(Va, Vb, Vc)**; a signal selection unit **(the component with ILp and ILn as outputs)** coupled with the region selection unit **(Region Selection Circuit)** and the

OCC core **(Low Pass Filters, multiplexers, comparators, flip-flops)** and configured to select one or more input signals based on the region of operation and provide the selected signals to the core **(Low Pass Filters, multiplexers, comparators, flip-flops)**; and a drive signal distribution unit **(LOGIC)** coupled to the OCC core **(Low Pass Filters, multiplexers, comparators, flip-flops)** and the region selection unit **(Region Selection Circuit)**. However Smedley et al. do not disclose the drive signal distribution unit configured to distribute the drive signals to a static volt-ampere-reactive (VAR) compensator (SVC), wherein the drive signals are configured to control a plurality of switching elements in the SVC. Bergmann **(Abstract)** teaches the drive signal distribution unit configured to distribute the drive signals to a static volt-ampere-reactive (VAR) compensator (SVC), wherein the drive signals are configured to control a plurality of switching elements in the SVC.

Smedley et al. and Bergmann disclose three-phase power transmission networks. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the power converter in the three-phase system disclosed by Smedley et al. with the Static VAR Compensator taught by Bergmann for the purpose of increasing the balance in a three-phase power transmission network.

Regarding dependent claims 25 and 34: Smedley et al. disclose the universal controller further comprising a reference signal source unit configured to provide a reference signal to the control core **(col. 2, lines 22-30)**.

Regarding dependent claims 26 and 35: Smedley et al. disclose the universal controller wherein the signal selection unit **(the component with ILp and ILn as**

outputs) is configured to combine the reference signal with each of the time varying voltage signals and select one or more input signals from the combined signals.

16. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley et al. (USP 6,297,980 - cited in IDS) as applied to claim 37 above, in view of Jacobs et al. (USP 6,046,915).

Smedley et al. **(FIG 5)** disclose a first voltage source **(Va)** configured to output a first time-varying signal, wherein the first voltage source is inductively coupled to a first input node. However Smedley et al. do not disclose that a first switching element coupled between the first input node and a first output node; a second switching element coupled between the first input node and a second output node; a third switching element coupled between the second input node a the first output node; a fourth switching element coupled between the second input node and the second output node; a first capacitive element coupled between the first and the second output node; and a second capacitive element coupled between the second output node and a third output node, wherein the third voltage source is inductively coupled with the third output node and each time-varying voltage signal has substantially the same period and a different phase.

Jacobs et al. **(FIG 15)** teach a first switching element **(FIG 1521)** coupled between the first input node and a first output node; a second switching element **(FIG 1527)** coupled between the first input node and a second output node; a third switching element **(FIG 1525)** coupled between the second input node a the first output node; a

fourth switching element **(FIG 1525)** coupled between the second input node and the second output node; a first capacitive element **(FIG 1514)** coupled between the first and the second output node; and a second capacitive element **(FIG 1515)** coupled between the second output node and a third output node, wherein the third voltage source is inductively coupled with the third output node and each time-varying voltage signal has substantially the same period and a different phase.

Smedley et al. and Jacobs et al. disclose control circuits for three phase powerpower supply. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the inverter disclosed by Smedley et al. with the phase selection circuit for three phase power converter taught by Jacobs et al. to control the waveshapes highest, lowest, and intermediate voltage to reduce harmonics associated with three phase time-varying input current.

17. Claims 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley et al. (USP 6,297,980 - cited in IDS).

Regarding independent claim 40: Smedley et al. **(FIG 7)** disclose a three phase three level universal controller, comprising: a one cycle control (OCC) core **(Low Pass Filters, multiplexers, comparators, flip-flops)** configured to generate a plurality of drive signals **(plurality signals from LOGIC)**, the OCC core **(Low Pass Filters, multiplexers, comparators, flip-flops)** comprising: a signal adjustment unit **(the component with ILp and ILn as outputs)** configured to condition a plurality of input signals and output a first **(ILp or ILn)** and a second **(ILp or ILn)** conditioned signals; a

first integrator **(AV(S))** configured to integrate an output voltage signal from a power converter and output a first integrated signal; a first comparator **(38)** communicatively coupled with the second integrator and the signal adjustment unit **(the component with ILp and ILn as outputs)**, the first comparator **(38)** configured to compare the first conditioned signal with the second integrated signal and output a first compared signal; a second comparator **(41)** communicatively coupled with the first integrator **(AV(S))** and the signal adjustment unit **(the component with ILp and ILn as outputs)**, the second comparator **(41)** configured to compare the second conditioned signal with the first integrated signal and output a second compared signal; a first flip-flop **(first flip-flop)** communicatively coupled with the first comparator **(41)** and a clock signal generator **(CLK)** and configured to output a first drive signal; and a second flip-flop **(second flip-flop)** communicatively coupled with the first comparator **(41)** and a clock signal generator **(CLK)** and configured to output a second drive signal, wherein the first and second drive signals are configured to control the power converter.

However Smedley et al. do not disclose a second integrator configured to integrate the output voltage signal from the power converter and output a second integrated signal. It would have been obvious to one having ordinary skill in the art at the time the invention was made to create second integrator from the first integrator to integrate an output voltage signal from power converter and output another integrated signal, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Regarding dependent claim 41: Smedley et al. disclose the controller, wherein the first flip-flop and second flip-flops are S/R flip-flops **(first and second flip-flops)**.

Regarding dependent claim 42: Smedley et al. **(FIG 7)** disclose the controller further comprising: a region selection unit **(Region Selection Circuit)** configured to monitor a first **(Va)**, second **(Vb)** and third **(Vc)** time-varying voltage signal, each voltage signal having a different phase, and configured to determine a region of operation based on the three time-varying voltage signals; an signal selection unit **(the component with ILp and ILn as outputs)** coupled with the region selection unit **(Region Selection Circuit)** and the OCC core **(Low Pass Filters, multiplexers, comparators, flip-flops)** and configured to select a plurality of input signals based on the region of operation and provide the selected input signals to the core **(Low Pass Filters, multiplexers, comparators, flip-flops)**; and a drive signal distribution unit **(LOGIC)** coupled to the OCC core **(Low Pass Filters, multiplexers, comparators, flip-flops)** and the region selection unit **(Region Selection Circuit)**, the drive signal distribution unit **(LOGIC)** configured to distribute the drive signals to the power converter, wherein the drive signals are configured to control a plurality of switching elements in the power converter.

18. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smedley et al. (USP 6,297,980 - cited in IDS) as applied to claim 43 above, in view of Bergmann (USP 5,672,957).

Smedley et al. disclose the claimed invention except that the power converter is a static volt-ampere-reactive (VAR) compensator (SVC). Bergmann **(Abstract)** teaches the power converter is a static volt-ampere-reactive (VAR) compensator (SVC).

Smedley et al. and Bergmann disclose three-phase power transmission networks. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the power converter in the three-phase system disclosed by Smedley et al. with the Static VAR Compensator taught by Bergmann for the purpose of increasing the balance in a three-phase power transmission network.

Allowable Subject Matter

19. Claims 15-23 are allowed.

20. The following is an examiner's statement of reasons for allowance:

Claim 15 recites, inter alia, connecting the voltage signal having the lowest voltage to only the third output node when the dominant voltage signal is lower than the non-dominant voltage signals; connecting the voltage signal having the highest voltage to one of the first output node and the second output node during each sub-period where the dominant voltage signal is lower than the non-dominant voltage signals; connecting the voltage signal having the intermediate voltage to one of the second output node and the third output node during each sub-period where the dominant voltage signal is lower than the non-dominant voltage signals; connecting the voltage signal having the highest voltage to only the second output node when the dominant voltage signal is higher than the non-dominant voltage signals; connecting the voltage

signal having the lowest voltage to one of the first output node and the second output node during each sub-period where the dominant voltage signal is higher than the non-dominant voltage signals; and connecting the voltage signal having the intermediate voltage to one of the second output node and the third output node during each sub-period where the dominant voltage signal is higher than the non-dominant voltage signals.

The art of record does not disclose the above limitations, nor would it be obvious to modify the art of record so as to include either of the above limitations.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Singh et al. (NPL Document: IEE Proc-Gener. Transm. Distrib., Vol. 144, No. 6, November 1997; “Active Power Filter with Sliding Mode Control”) disclose an active power filter with sliding mode control, Dahler et al. (USP 5,793,622) disclose a power converter with three AC voltage sources inductively coupled to separate input nodes, Ooi (USP 4,941,079) discloses PWM power transmission system with conventional converter having static VAR controller SVC, and Oates (USP 6,879,062) discloses a substation in a power transmission network with 3-phase voltages and currents represented by sliding mode control technique.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EMILY PHAM whose telephone number is (571)270-3046. The examiner can normally be reached on Mon-Thu (7:00AM - 6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm Ullah can be reached on (571) 272 - 2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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